Session-01

Introduction to Analog and Mixed Signal Circuit Design

Session delivered by:

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Session Objectives

✓ To understanding the concepts of
  – Introduction to analog circuit design
  – Characteristics of analog circuit
  – Principle, concept and techniques
  – Trade off
  – Challenges and assumption
  – Application area and future of analog IC
✓ To understand and design sub blocks of analog circuits design
✓ To understand the MOS transistor in analog circuits
✓ To understand the concept of current mirrors and current sources/sinks
✓ To design current mirrors and current sources/sinks
✓ To model and simulate the current mirror using Hspice/Cadence Virtuosos
Session Topics

✓ Introduction to analog and mixed signal circuit circuit design
✓ Analog IC design Process and Characteristics of analog circuit
✓ Principle, concept and techniques of analog circuit
✓ Hierarchy
✓ Trade off
✓ Challenges and assumption
✓ Application area and future of analog IC
✓ MOS transistor in analog circuits
✓ Introduction to current mirror
✓ Types of Current mirrors
✓ Design of Current mirror
✓ Simulation of Current mirror
✓ Analysis of current mirror
Introduction

This course teaches analog and mixed signal integrated circuit design using CMOS technology.
Course Philosophy

✓ Think before design
Analog Circuit Design

Definition

✓ Design – To create or execute in an artistic or highly skilled manner. The invention and disposition of the forms, parts, or details of something according to a plan

Analysis versus Synthesis (Design)

- **Analysis**: Given a system, find its properties. The solution is unique.
- **Design**: Given a set of properties, find a system possessing them. The solution is rarely unique
The Analog IC Design Process

Conception of the idea

Definition of the design

Implementation

Simulation

Physical Definition

Physical Verification

Parasitic Extraction

Fabrication

Testing and Verification

Product
Electrical Design

Electrical design is the process of going from the specifications to a circuit solution. The inputs and outputs of electrical design are:

1. Circuit or systems specifications
2. Analog Integrated Circuit Design
3. Topology
4. DC currents

The electrical design requires active and passive device electrical models for:

- Creating the design
- Verifying the design
- Determining the robustness of the design
Steps in Electrical Design

✓ Selection of a solution
  – Examine previous designs
  – Select a solution that is simple
✓ Investigate the solution
  – Analyze the performance (without a computer)
  – Determine the strengths and weaknesses of the solution
✓ Modification of the solution
  – Use the key principles, concepts and techniques to implement
  – Evaluate the modifications through analysis (still no computers)
✓ Verification of the solution
  – Use a simulator with precise models and verify the Solution
  – Large disagreements with the hand analysis and computer verification should be carefully examined
Physical Design

Physical design is the process of representing the electrical design in a layout consisting of many distinct geometrical rectangles at various levels. The layout is then used to create the actual, three-dimensional integrated circuit through a process called fabrication.
Layout Process

✔ The inputs are the W/L values and the schematic (generally from schematic entry used for simulation)

✔ A CAD tool is used to enter the various geometries. The designer must enter the location, shape, and level of the particular geometry

✔ During the layout, the designer must obey a set of rules called design rules. These rules are for the purpose of ensuring the robustness and reliability of the technology

✔ Once the layout is complete, then a process called layout versus schematic (LVS) is applied to determine if the physical layout represents the electrical schematic

✔ The next step is now that the physical dimensions of the design are known, the parasitics can be extracted. These parasitics primarily include:
  - Capacitance from a conductor to ground
  - Capacitance between conductors
  - Bulk resistance

✔ The extracted parasitics are entered into the simulated database and the design is resimulated to insure that the parasitics will not cause the design to fail.
Packaging

✓ Packaging of the integrated circuit is an important part of the physical design process. The function of packaging is:

– Protect the integrated circuit
– Power the integrated circuit
– Cool the integrated circuit
– Provide the electrical and mechanical connection between the integrated circuit and the outside world

✓ Packaging steps

- Dicing the wafer
- Attachment of the chip to a lead frame
- Connecting the chip to a lead frame
- Encapsulating the chip and lead frame in a package

✓ Other considerations of packaging:

– Speed
– Parasitics (capacitive and inductive)
Test Design

✓ Test design is the process of coordinating, planning and implementing the measurement of the analog integrated circuit performance

✓ **Objective**: To compare the experimental performance with the specifications and/or simulation results

✓ Types of tests

  – Functional: verification of the nominal specifications
  – Parametric: verification of the characteristics to within a specified tolerance
  – Static: verification of the static (AC and DC) characteristics of a circuit or system
  – Dynamic: verification of the dynamic (transient) characteristics of a circuit or system

✓ Additional Considerations:

  – Should the testing be done at the wafer level or package level?
  – How do you remove the influence (de-embed) of the measurement system from the measurement?
Characteristics of Analog Integrated Circuit Design

✓ Done at the circuits level
✓ Complexity is high
✓ Continues to provide challenges as technology evolves
✓ Demands a strong understanding of the principles, concepts and techniques
✓ Good designers generally have a good physics background
✓ Must be able to make appropriate simplifications and assumptions
✓ Requires a good grasp of both modeling and technology
✓ Have a wide range of skills - breadth (analog only is rare)
✓ Be able to learn from failure
✓ Be able to use simulation correctly
Complexity in Analog Design

- Analog design is normally done in a non-hierarchical manner and makes little use of repeated blocks. As a consequence, analog design can become quite complex and challenging.

- How do you handle the complexity?
  - Use as much hierarchy as possible
  - Use appropriate organization techniques
  - Document the design in an efficient manner
  - Make use of assumptions and simplifications
  - Use simulators appropriately
Trends in Analog IC Design

✓ Analog IC Design has Reached Maturity
✓ There are established fields of application
  – Digital-analog and analog-digital conversion
  – Disk drive controllers
  – Modems – filters
  – Bandgap reference
  – Analog phase lock loops
  – DC-DC conversion
  – Buffers and
  – Codecs, etc.,
✓ Existing philosophy regarding analog circuits
  – “If it can be done economically by digital, don’t use analog.”
✓ Consequently
  – Analog finds applications where speed, area, or power have advantages over a digital approach.
Analog IC Design Challenges

Technology:

✓ Digital circuits have scaled well with technology
✓ Analog does not benefit as much from smaller features
  – Speed increases
  – Gain decreases
  – Matching decreases
  – Nonlinearity increases
  – New issues appear such as gate current leakage

Analog Circuit Challenges:

✓ Trade offs are necessary between linearity, speed, precision and power
✓ As analog is combined with more digital, substrate interference will become worse
Trade offs between linearity, speed, precision and power

![Graphs showing trade-offs](image-url)
Hierarchy of Analog and Mixed Signal Circuit Design

- Systems Level (ADC)
- Circuits Level (op amps)
- Block Level (amplifier)
- Sub-block Level (current sink)
- Components Level (transistor)
Example of Hierarchy in Analog Circuits
Current Voltage (IV) Plots

✓ (DC) current-voltage characteristics of a resistor, a current source, and a voltage source shown in Fig 1

Often the controlling parameter in a semiconductor device is a voltage. The controlled parameter is then the device's output current

✓ The resistance can be calculated by taking the reciprocal of the IV plot slope

✓ The voltage source in this figure has zero resistance; the current source, infinite resistance.
The slope of the resistor is 200 nA/1 V. The resistance value is the reciprocal of this slope (5MEG)
MOS Transistor in Analog Design

✓ MOSFET looks like a resistor when operating in the linear region
✓ MOSFET looks like a current source when operating in the saturation region

In the saturation region, the MOSFET behaves, like a current source in parallel with a resistor if consider the channel length modulation

✓ The resistive component, whether in the triode or saturation regions, is often called the MOSFET's output resistance
MOS Transistor in Analog Design

✓ MOSFET's output resistance \( r_o \) is

\[
r_o = \frac{1}{\lambda I_{D,sat}}
\]

✓ \( V_{ds,sat} \) term is very important and will be used frequently when doing analog design.

✓ The amount of gate-source voltage that we have in excess or over the threshold voltage called as \( V_{DS,Sat} = \text{excess gate voltage} = \text{gate overdrive voltage} \)

✓ In analog design, for the MOSFET to operate in the saturation region gate and drain to be connected

\[+\]
\[\begin{array}{c}
\text{+} \\
V_{GS} \\
\text{+} \\
\text{ID} \\
V_{DS} \\
\text{+} \\
\text{ID} \\
\text{+} \\
\text{+} \\
\text{+} \\
\text{+} \\
\text{+} \\
\end{array}\]
Movement of V and I in MOS

✓ Imagine injecting a current into the drain of the NMOS device.

✓ What happens to the device's drain current?
  - ANSWER
    • it goes up

✓ What happens to the device's $V_{DS}$?
  - ANSWER
    • it goes up
Movement of V and I in NMOS

✓ Stealing current from the NMOS's drain

What happens to the device's drain current?

– ANSWER
  • it goes down

What happens to the device's VDS?

– ANSWER
  • it goes down
Movement of V and I in PMOS

✓ injecting a current into the drain

What happens to the device's drain current?

– ANSWER
  • it goes down

What happens to the device's VDS?

– ANSWER
  • it decreases (drain voltage moves towards the power supply VDD)
Movement of V and I in PMOS

✓ steeling a current from the drain

✓ What happens to the device's drain current?
  
  – ANSWER
    • it increases

✓ What happens to the device's \( V_{DS} \)?

  – ANSWER
    • drain voltage will move towards ground
Small Signal Models

- In analog circuits, input signal containing both AC and DC components

AC component is our analog signal to be processed and DC component is for biasing the transistor.

Small-signal models are used to calculate AC gains
Small Signal Models

✓ We adjust the DC gate-source voltage, $V_{GS}$, to a value that corresponds to a DC drain current $I_D$.

✓ At this bias point, we apply a small AC signal where $|V_{gs}| << |V_{GS}|$ and $|i_d| << |I_D|$. Because the signals are small, the change in drain current, $i_d$, with gate voltage, $v_{gs}$ is essentially linear.

If our AC signal amplitudes get comparable to the DC operating (or bias) points, we get high nonlinearity (which makes feedback necessary for any highly linear amplifier).
An extremely important parameter in analog design is a device's transconductance, $g_m$

$g_m$ of a device is an AC small-signal parameter that relates the AC gate voltage to the AC drain current, that is, $i_d = g_m v_{gs}$

$g_m$ is simply the slope of the line at the intersection of the DC operating values $V_{GS}$ and $I_D$.

$$i_D = i_d + I_D = \frac{KP_n}{2} \cdot \frac{W}{L} \cdot \left( \frac{v_{GS}}{v_{gs} + V_{GS} - V_{THN}} \right)^2$$

To find the slope ($g_m$) of the $i_D-v_{GS}$ curve at the fixed bias points $V_{GS}$ and $I_D$

$$g_m = \left[ \frac{\delta i_D}{\delta v_{GS}} \right]_{v_{GS} = \text{constant}}^{i_D = \text{constant}} = KP_n \cdot \frac{W}{L} \cdot (v_{gs} + V_{GS} - V_{THN})$$

$$\beta_n = KP_n \cdot \frac{W}{L} \quad \text{and} \quad |v_{gs}| \ll V_{GS} \quad \therefore \quad g_m = \frac{V_{DS,sat}}{V_{GS} - V_{THN}} = \sqrt{2\beta_n I_D}$$
Body Effect Transconductance, $g_{mb}$

- The drain current varies with source-to-bulk potential $V_{SB}$.
- If we raise the potential of the source, we eventually run into the point where the source potential is less than a $V_{THN}$ below the gate potential, and the MOSFET shuts off.

$V_G > V_{SB} + V_{THN}$ for the MOSFET to be on.

MOSFET shuts off because source potential gets too large.
**Body Effect Transconductance, \( g_{mb} \)**

- The body-effect is the variation of the threshold voltage with \( V_{SB} \).

\[
g_{mb} = \left[ \frac{\partial i_D}{\partial V_{SB}} \right]_{V_{SB} = \text{constant}} = \frac{\partial}{\partial V_{SB}} \left[ \frac{K P_n}{2} \cdot \frac{W}{L} (V_{GS} - V_{THN})^2 \right]_{V_{SB} = \text{constant}}
\]

\[
g_{mb} = g_m \cdot \eta
\]

- The factor \( \eta \) describes how the threshold voltage changes with \( V_{SB} \) and generally ranges from 0 (no body effect) to 0.5.
Output Resistance

\[ r_0^{-1} = \left[ \frac{\partial i_D}{\partial v_{DS}} \right]_{v_{DS} = \text{constant}} \frac{I_D = \text{constant}}{= \frac{\partial}{\partial v_{DS}} \left( \frac{K P_n}{2} \cdot \frac{W}{L} (V_{GS} - V_{THN})^2 \left( 1 + \lambda \left( \frac{v_{DS}}{v_{ds} + V_{DS} - V_{DS,sat}} \right) \right) \right)} \]

\[ i_D = I_D + i_d \]

\[ V_{GS} \]

\[ V_{DS} \]

\[ v_{ds} \]

\[ 0 \quad V_{DS} \quad v_{DS} \]

\[ r_0 = \frac{1}{\lambda I_{D,sat}} \]

One over the slope is output resistance.
Output Resistance

\[ r_O = \frac{\partial V_{DS}}{\partial I_D} \]

\[ = \frac{1}{\frac{\partial I_D}{\partial V_{DS}}} \cdot \]

\[ = \frac{1}{\frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \cdot \lambda} \cdot \]

\[ \approx \frac{1}{\lambda I_D}. \]
Output Resistance

\[ I_{DS} = K_n' \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \]

\[ r_{DS} = r_o = \frac{V_{EL}}{I_{DS}} \]

\[ \lambda = \frac{1}{V_{EL}} \]

\[ V_{En} = 4 \text{V/\mu mL} \]

\[ L = 1 \mu m \]

\[ I_{DS} = 100 \mu A \]

\[ r_o = 40 \text{k}\Omega \]
Determine $\lambda$

- The $V_{GS}$ (NMOS) and $V_{SG}$ (PMOS) of the MOSFETs are 1.05 V and 1.15 V, respectively (roughly for 20 uA of bias current).

\[
\lambda_n = \frac{1}{I_{D,sat} \cdot r_o} = \frac{1}{20\mu \cdot 5MEG} = 0.01 \ V^{-1}
\]

\[
\lambda_p = \frac{1}{20\mu \cdot 4MEG} = 0.0125 \ V^{-1}
\]

\[
I_{D,sat} = \frac{K_P N}{2} \cdot \frac{W}{L} \cdot V_{DS,sat}^2
\]

\[
\lambda \propto \frac{1}{L}
\]

\[
r_o \propto \frac{L^2}{V_{DS,sat}^2}
\]
Output Resistance

\[ V_{GS} = 1.05 \, \text{V} \]

\[ V_{SG} = 1.15 \, \text{V} \]
MOSFET Transition Frequency, \( f_T \)

- The drain of the MOSFET is at AC ground (shorted through the DC drain-source voltage).

- This causes, from the gate terminal, \( C_{gs} \) and \( C_{gd} \) to appear as though they are in parallel.

\[
v_{gs} = \frac{i_g}{j\omega \cdot (C_{gs} + C_{gd})}
\]

- Knowing \( i_d = g_m \cdot v_{gs} \), we can write the current gain of the MOSFET as
MOSFET Transition Frequency, $f_T$

- The frequency where the current gain of the MOSFET is one, the transition frequency, $f_T$ (the transistor transitions from an amplifier to an attenuator)

$$ C_{gs} \left( = \frac{2}{3} W L C_{ox}' \right) \gg C_{gd}, $$

$$ f_T \approx \frac{g_m}{2 \pi C_{gs}} = \frac{3 K P_n \cdot (V_{GS} - V_{THN})}{4 \pi \cdot L^2 C_{ox}'} = \frac{3 \mu_n}{4 \pi} \cdot \frac{V_{DS,sat}}{L^2} $$

- To get high speed, we need to use minimum channel lengths and design with a large $V_{DS}$

- Minimum lengths results in lower output resistances, lower gain (higher speed resulting in lower gain)

- A large $V_{DS,Sat}$, the MOSFETs enter the triode region earlier (resulting in reduced output swing in amplifiers or mirrors)
MOSFET Transition Frequency, $f_T$

✔ For short-channel devices, the mobility is no longer constant but starts to decrease (velocity saturation) with decreasing length (increasing electric field between the drain and channel).

✔ the term $\mu_n/L$ as a relatively constant value

$$f_T \propto \frac{V_{DS,\text{Sat}}}{L} \quad \text{(Short-channel devices)}$$

✔ For high-speed, to use the smallest possible channel length and large $V_{DS,\text{Sat}}$
Device Sizes for Analog Design

\[ r_o \propto \frac{L^2}{V_{\text{DS, sat}}^2} \]

\[ f_T \approx \frac{g_m}{2\pi C_{gs}} = \frac{3K_P n \cdot (V_{GS} - V_{\text{THN}})}{4\pi \cdot L^2 C'_{ox}} = \frac{3\mu_n}{4\pi} \cdot \frac{V_{\text{DS, sat}}}{L^2} \]

✓ For general analog design, use an \( L \) of 2-5 times minimum

✓ Use \( L \), for analog design, of 2 as a good trade-off between speed and gain.

✓ For general design, use a \( V_{\text{DS, sat}} \) of 5% of VDD
# MOS Model for Analog Design

<table>
<thead>
<tr>
<th>Parameter</th>
<th>NMOS</th>
<th>PMOS</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bias current, $I_D$</td>
<td>20 $\mu$A</td>
<td>20 $\mu$A</td>
<td>Approximate</td>
</tr>
<tr>
<td>$W/L$</td>
<td>10/2</td>
<td>30/2</td>
<td>Selected based on $I_D$ and $V_{DS, sat}$</td>
</tr>
<tr>
<td>$V_{DS, sat}$ and $V_{SD, sat}$</td>
<td>250 mV</td>
<td>250 mV</td>
<td>For sizes listed</td>
</tr>
<tr>
<td>$V_{GS}$ and $V_{SG}$</td>
<td>1.05 V</td>
<td>1.15 V</td>
<td>No body effect</td>
</tr>
<tr>
<td>$V_{THN}$ and $V_{THP}$</td>
<td>800 mV</td>
<td>900 mV</td>
<td>Typical</td>
</tr>
<tr>
<td>$\partial V_{THN,P} / \partial T$</td>
<td>$-1$ mV/Cº</td>
<td>$-1.4$ mV/Cº</td>
<td>Change with temperature</td>
</tr>
<tr>
<td>$KP_n$ and $KP_p$</td>
<td>120 $\mu$A/V²</td>
<td>40 $\mu$A/V²</td>
<td>$t_{ox} = 200$ Å</td>
</tr>
<tr>
<td>$C'<em>{ox} = \varepsilon</em>{ox} / t_{ox}$</td>
<td>1.75 fF/µm²</td>
<td>1.75 fF/µm²</td>
<td>$C_{ox} = C'_{ox} WL \cdot (\text{scale})^2$</td>
</tr>
<tr>
<td>$C_{oxn}$ and $C_{exp}$</td>
<td>35 fF</td>
<td>105 fF</td>
<td>PMOS is three times wider</td>
</tr>
<tr>
<td>$C_{gsn}$ and $C_{sgp}$</td>
<td>23.3 fF</td>
<td>70 fF</td>
<td>$C_{gs} = \frac{2}{3} C_{ox}$</td>
</tr>
<tr>
<td>$C_{gdn}$ and $C_{dgp}$</td>
<td>2 fF</td>
<td>6 fF</td>
<td>$C_{gd} = CGDO \cdot W \cdot \text{scale}$</td>
</tr>
<tr>
<td>$g_{mn}$ and $g_{mp}$</td>
<td>150 $\mu$A/V</td>
<td>150 $\mu$A/V</td>
<td>At $I_D = 20$ $\mu$A</td>
</tr>
<tr>
<td>$r_{on}$ and $r_{op}$</td>
<td>5 MΩ</td>
<td>4 MΩ</td>
<td>Approximate at $I_D = 20$ $\mu$A</td>
</tr>
<tr>
<td>$g_{mn} r_{on}$ and $g_{mp} r_{op}$</td>
<td>750 V/V</td>
<td>600 V/V</td>
<td>Open circuit gain</td>
</tr>
<tr>
<td>$\lambda_n$ and $\lambda_p$</td>
<td>0.01 V⁻¹</td>
<td>0.0125 V⁻¹</td>
<td>At $L = 2$</td>
</tr>
<tr>
<td>$f_{In}$ and $f_{Ip}$</td>
<td>900 MHz</td>
<td>300 MHz</td>
<td>For $L = 2$, $f_I$ goes up if $L = 1$</td>
</tr>
</tbody>
</table>

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# MOS Model for Analog Design

**Short-channel MOSFET parameters for general analog design**

\[ VDD = 1 \text{ V and a scale factor of 50 nm (scale = 50e}^{-9}) \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>NMOS</th>
<th>PMOS</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bias current, ( I_D )</td>
<td>10 ( \mu )A</td>
<td>10 ( \mu )A</td>
<td>Approximate, see Fig. 9.31</td>
</tr>
<tr>
<td>( W/L )</td>
<td>50/2</td>
<td>100/2</td>
<td>Selected based on ( I_D ) and ( V_{ov} )</td>
</tr>
<tr>
<td>Actual ( W/L )</td>
<td>2.5 ( \mu )m/100nm</td>
<td>5 ( \mu )m/100nm</td>
<td>( L_{min} ) is 50 nm</td>
</tr>
<tr>
<td>( V_{DS, sat} ) and ( V_{SD, sat} )</td>
<td>50 mV</td>
<td>50 mV</td>
<td>However, see Fig. 9.32 and the associated discussion</td>
</tr>
<tr>
<td>( V_{GS} ) and ( V_{SG} )</td>
<td>350 mV</td>
<td>350 mV</td>
<td>No body effect</td>
</tr>
<tr>
<td>( V_{THN} ) and ( V_{THP} )</td>
<td>280 mV</td>
<td>280 mV</td>
<td>Typical</td>
</tr>
<tr>
<td>( \delta V_{THN,P}/\delta T )</td>
<td>(- 0.6 \text{ mV/C}^\circ)</td>
<td>(- 0.6 \text{ mV/C}^\circ)</td>
<td>Change with temperature</td>
</tr>
<tr>
<td>( v_{sat} ) and ( v_{sat} )</td>
<td>(110 \times 10^3 \text{ m/s} )</td>
<td>(90 \times 10^3 \text{ m/s} )</td>
<td>From the BSIM4 model</td>
</tr>
<tr>
<td>( t_{ox} )</td>
<td>14 ( \AA )</td>
<td>14 ( \AA )</td>
<td>Tunnel gate current, 5 A/cm(^2)</td>
</tr>
<tr>
<td>( C'<em>{ox} = \varepsilon</em>{ox}/t_{ox} )</td>
<td>25 ( f )F/( \mu )m(^2)</td>
<td>25 ( f )F/( \mu )m(^2)</td>
<td>( C_{ox} = C'_{ox} W L \cdot (\text{scale})^2 )</td>
</tr>
<tr>
<td>( C_{oxn} ) and ( C_{oxp} )</td>
<td>6.25 ( f )F</td>
<td>12.5 ( f )F</td>
<td>PMOS is two times wider</td>
</tr>
<tr>
<td>( C_{gsn} ) and ( C_{gsp} )</td>
<td>4.17 ( f )F</td>
<td>8.34 ( f )F</td>
<td>( C_{gs} = \frac{2}{3} C_{ox} )</td>
</tr>
<tr>
<td>( C_{gdn} ) and ( C_{dgp} )</td>
<td>1.56 ( f )F</td>
<td>3.7 ( f )F</td>
<td>( C_{gd} = CGDO \cdot W \cdot \text{scale} )</td>
</tr>
<tr>
<td>( g_{m,n} ) and ( g_{m,p} )</td>
<td>150 ( \mu )A/V</td>
<td>150 ( \mu )A/V</td>
<td>At ( I_D = 10 \mu )A</td>
</tr>
<tr>
<td>( r_{on} ) and ( r_{off} )</td>
<td>167 k( \Omega )</td>
<td>333 k( \Omega )</td>
<td>Approximate at ( I_D = 10 \mu )A</td>
</tr>
<tr>
<td>( g_{m,n} r_{on} ) and ( g_{m,p} r_{op} )</td>
<td>25 V/V</td>
<td>50 V/V</td>
<td>!!Open circuit gain!!</td>
</tr>
<tr>
<td>( \lambda_n ) and ( \lambda_p )</td>
<td>0.6 V(^{-1})</td>
<td>0.3 V(^{-1})</td>
<td>( L = 2 )</td>
</tr>
<tr>
<td>( f_{IH} ) and ( f_{TP} )</td>
<td>6000 MHz</td>
<td>3000 MHz</td>
<td>Approximate at ( L = 2 )</td>
</tr>
</tbody>
</table>
Current Mirror

✓ Application
  – Biasing element
  – Load devices for amplifier

✓ Use of CM in biasing can result in superior insensitivity of circuit performance to variations in power supply and temperature

✓ Current mirrors are more economical than resistors in terms of the die area required to provide bias current of a certain value, particularly when the required value of bias current is small

✓ When used as a load element in transistor amplifiers, the high incremental resistance of the current mirror results in the high voltage gain at low power supply voltages
Biaseding

✓ How should a MOSFET be biased so as to operate as a stable current source?

This expression reveals various dependencies of $I_{out}$ upon the supply, process, and temperature.

✓ The overdrive voltage is a function of $V_{DD}$ and $V_{Th}$, the threshold voltage may vary by 100 mV from wafer to wafer.
Current Source

✓ The design of current sources in analog circuits is based on "copying" currents from a reference, with the assumption that one precisely-defined current source is already available.

✓ How do we generate copies of a reference current? How do we guarantee \( I_{\text{out}} = I_{\text{REF}} \)?
The structure consisting of $M_1$ and $M_2$ in fig is called a "current mirror"

\[ I_{REF} = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right)_1 (V_{GS} - V_{TH})^2 \]

\[ I_{out} = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right)_2 (V_{GS} - V_{TH})^2, \]

\[ I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}. \]
Simple Current Mirror

\[ I_{D1} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS1}) \]

\[ I_{D2} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS2}), \]

\[ \frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}. \]

While \( V_{Dsl} = V_{Gsl} = V_{GS2} \), \( V_{DS2} \) may not equal \( V_{GS2} \) because of the circuitry fed by M2,
Importance of Cascode Stages

- Increasing output resistance by increasing the device length or Cascoding

- That the high output impedance arises from the fact that if the output node voltage is changed by $\Delta V$, the resulting change at the source of the cascode device is much less.

- In a sense, the cascode transistor "shields" the input device from voltage variations at the output. The shielding property of cascodes proves useful in many circuits.
Cascode Current Source

✓ In order to suppress the effect of channel-length modulation, a cascode current source can be used

✓ If \( V_b \) is chosen such that \( V_y = V_x \), then \( I_{out} \) closely tracks \( I_{REF} \)

✓ The cascode device "shields" the bottom transistor from variations in \( V_p \)
Cascode Current Mirror
Cascode Current Mirror

✓ How do we generate V
✓ to ensure V_y = V_x, we must guarantee V_b - V_{GS3} = V_X \text{ or } V_b = V_{GS3} + V_X
✓ V_X. This result suggests that if a gate-source voltage is added to V_x, the required value of V_b can be obtained
✓ The idea is to place another diode-connected device, M_0, in series with M_1, thereby generating a voltage V_N = V_{GSO} + V_X
✓ Proper choice of the dimensions of M_0 with respect to those of M_3 yields V_{GSO} = V_{GS3}
✓ Connecting node N to the gate of M_3, we have V_{GSO} + V_x = V_{GS3} + V_Y
✓ Thus, if (W/L)_3/(W/L)_0 = (W/L)_2/(W/L)_1, then V_{GS3} = V_{GSO} and V_x = V_y
Simple MOS Current Mirror

Assume transistors in active region, \( \lambda = 0 \), and same size

\[ I_{out} = I_{in} \]

\[ i_y = \frac{v_y}{r_{ds1}} + g_{m1} v_y \Rightarrow \frac{v_y}{i_y} = r_{ds1} \parallel \frac{1}{g_{m1}} \approx \frac{1}{g_{m1}} \]
Simple CMOS Current Mirror

Small Signal Equivalent Circuit (Low Frequency)
Simple CMOS Current Mirror

Design a current mirror such that $V_{eff}$ is > 0.5 V and $r_{out}$ > 300 kΩ at an input current of 100μA.

Given: $\mu_n C_{ox} = 92 \mu A/V^2$; $V_{in} = 0.8$ V;
$r_{ds} = 1/\lambda I_D = 8000L(\mu m)/I_D (mA)$

Solution:

$r_{out} = r_{ds} = \frac{1}{\lambda I_D} = \frac{8000L(\mu m)}{I_D (mA)} > 300 \text{ kΩ} \Rightarrow L > \frac{300 \text{ kΩ} \cdot 0.1}{8000} = 3.75 \mu m$

$\Rightarrow L = 4 \mu m$

$I_D = \frac{\mu_n C_{ox} W}{2 L} V_{eff}^2 \Rightarrow W < \frac{100 \mu A \cdot 2 \cdot 4 \mu m}{92 \mu A \cdot 0.25 V^2} = 34.8 \mu m$

$\Rightarrow W = 34 \mu m$
Cascode Current Mirror

![Graph showing current mirror characteristics](image)

- $i_T = 60 \mu A$
- $i_T = 50 \mu A$
- $i_T = 40 \mu A$
- $i_T = 30 \mu A$
- $i_T = 20 \mu A$
- $i_T = 10 \mu A$

**MODEL**
- MNMOS1 NMOS VTC=0.75 KP=25U
- $\lambda$ = 0.01 GAMMA=0.8 PHI=0.6
- M1 1 1 0 0 MNMOS1 W=3U L=3U
- M2 2 1 0 0 MNMOS1 W=3U L=3U
- M3 3 3 1 0 MNMOS1 W=3U L=3U
- M4 4 3 2 0 MNMOS1 W=3U L=3U

**VOUT**
- 40uA, 60uA

**iOUT**
- 0, 20uA, 40uA, 60uA
Simple Current Mirror Design

- Design a NMOS based current mirror which can sink/mirror a current of 30µA. Estimate the output resistance. Also find the device dimensions in order to mirror 30µA of current.

Solution:

Assume $V_{GS} = 0.7V$

The value of $R$, can be found by assuming $I_{D1} = I_{D2} = 30µA$, is determined by solving the equation below

$$I_{D1} = \frac{V_{DD} - V_{DS}}{R}$$

$$\Rightarrow R = \frac{V_{DD} - V_{DS}}{I_{D1}} = \frac{1.8 - 0.7}{30µ} = 36.66KΩ$$
Simple Current Mirror Design

Solving for the width of the transistors, since the transistors operate in saturation region

\[ I_{D2} = 30 \mu A = \frac{K_n W}{2 L} (V_{GS} - V_{TH})^2 \]

\[ 30 \mu A = 1655 \times \frac{W}{L} \times (0.7 - 0.37992)^2 \]

\[ \frac{W}{L} = 1.769 \]

Let \( L_1 = L_2 = 0.36 \mu m \), then \( W_2 = 0.636 \mu m \), which gives \( W_1 = 0.636 \mu m \)

The small signal output resistance of the current source is given by

\[ r_o = \frac{1}{\lambda I_o} = \frac{1}{0.09 \times 30 \mu A} = 0.37 \, M\Omega \]
Simple Current Mirror Design

✓ SPICE code

NMOS Current Source / Current Mirror

.include "C:\synopsys\FT07Analog\modelfile018.txt"

R1 Vdd P1 32.5K
M1 P1 P1 gnd gnd CMOSN L=0.36U W=0.7U
M2 P2 P1 gnd gnd CMOSN L=0.36U W=0.7U

Vdd Vdd gnd dc 1.8
V2 P2 gnd dc 0
.dc V2 0 1.8 0.01
.op
.print dc i(M1) i(M2) v(P2) i(R1)
.end
Simple Current Mirror Design

✓ Simulation Results
Cascode Current Mirror

✓ Design a cascode current source with a DC output current of 50µA and a small signal output resistance of 100MΩ.

Solution

Begin the design by setting the gate voltage of M₁ and M₃ to ensure that M₂ and M₄ are operating in their constant current region with $V_{D4}=0.5\text{V}$

Let $V_{GS}$ of M₁, M₂, M₃ and M₄ be 0.8V, the gate voltage on M₄ will be 1.6V

With $V_{GS4}=0.8\text{V}$, it implies that the source of M₄, which is the drain of M₂ will be at 0.8V
Cascode Current Mirror

Since $V_{DS2} = 0.8V$,
Recalling that $V_{GS2} - V_{Tn} = 0.8 - 0.379924 = 0.420076V$,

Note that $V_{DS(Sat)4} = 0.8V$ the source of $M_4$ is at 0.8V, the drain voltage must be greater than 0.5V to ensure operation in the constant current region.

Setting the W/L ratio of $M_1$ and $M_3$ to yield $V_{GS} = 0.8V$ with $I_{ref} = 50\mu A$

\[
V_{GS} = V_{Tn} + \sqrt{\frac{I_{REF}}{W \mu_n C_{ox}}} + \frac{0.8}{0.379924} + \sqrt{\frac{50}{W \times L}}
\]

\[
\frac{W}{L} = 1.712
\]

\[
\frac{W_1}{L_1} = \frac{W_3}{L_3} = 1.712
\]
Cascode Current Mirror

We can match the (W/L) of M2 and M4 with M1 and M3, respectively, since we want $I_{\text{REF}} = I_{\text{OUT}}$

$$\therefore \frac{W_2}{L_2} = \frac{W_4}{L_4} = 1.712$$

To calculate the small signal output resistance

$$R_S = (g_{m4} \cdot r_{o4})r_{o2}$$

$$r_{o4} = r_{o2} = \frac{1}{\lambda_n I_D}$$

$$r_{o4} = r_{o2} = \frac{1}{0.09 \times 50 \mu} = 0.22\,\text{M}\Omega$$

$$g_{m4} = \sqrt{2 \frac{W}{L} \mu_n C_{ox} I_{\text{REF}}} = \sqrt{4 \times 1.712 \times 165.5 \times 50} = 238.04$$

$$R_S = (g_{m4} \cdot r_{o4})r_{o2} = 238.04 \times 0.22 \times 0.22 = 11.52\,\text{M}\Omega$$
Cascode Current Mirror

✓ SPICE code

Cascode Current Mirror

M1 P3 P3 Gnd Gnd CMOSN L=0.7U W=1.2U
M2 P4 P3 Gnd Gnd CMOSN L=0.7U W=1.2U
M3 P1 P1 P3 Gnd CMOSN L=0.7U W=1.2U
M4 P2 P1 P4 Gnd CMOSN L=0.7U W=1.2U

I1 Vdd P1 dc 50u
Vdd Vdd Gnd dc 1.8V
V1 P2 gnd dc 0.5V

.dc V1 0 1.8 0.01
.Print dc i(M1) i(M2) i(M3) i(M4)
.end
✓ Simulation Results
Summary

- Successful analog IC design proceeds with understanding the circuit before simulation.

- Analog IC design consists of three major steps:
  - Electrical design (Topology, W/L values, and dc currents)
  - Physical design (Layout)
  - Test design (Testing)

- Analog designers must be flexible and have a skill set that allows one to simplify and understand a complex problem.

- The appropriate philosophy is “If it can be done economically by digital, don’t use analog.”

- As a result of the above, analog finds applications where speed, area, or power have advantages over a digital approach.

- Deep-submicron technologies will offer exciting challenges to the creativity of the analog designer.
Summary

✓ MOSFET looks like a resistor when operating in the linear region
✓ MOSFET looks like a current source when operating in the saturation region
✓ Small-signal models are used to calculate AC gains
✓ Current mirrors are used as current references and as load circuits
Summary

✓ A current mirror is characterized by
  – The independence of the output current on the voltage across it ($r_{out}$ - large)
  – The output voltage range over which output current is dependent (VMIN (out))
  – The independence of the input voltage on the input current ($r_{in}$ - small)
  – The range of input voltage over which the input current is independent (VMIN(in))
  – The accuracy of the current out as a function of the current in ratio

✓ A voltage or current reference is independent of power supply