Session 2
MOS Transistor for RF Circuits

Session Speaker
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Session Contents

- MOS transistor basics
- MOS equivalent circuit
- Single stage amplifiers
- Opamp design
Session objectives

• To understand the MOS device characteristics
• To derive MOS equivalent circuit and understand small signal model
• To design and analyze single stage amplifiers and Opamp
MOS I/V Characteristics

Threshold voltage

Derivation of I/V characteristics
MOS I/V Characteristics: Threshold Voltage (1)

"Threshold voltage" ($V_{TH}$) - The value of $V_{GS}$ for at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the threshold voltage. $V_{TH}$ is given by:

$$V_{TH} = \Phi_{MS} + 2\Phi_{F} + \frac{Q_{dep}}{C_{ox}},$$

where

$\Phi_{MS}$ - the difference between the work functions of the polysilicon gate and the silicon substrate,

$\Phi_{F} = (KT/q) \ln(N_{sub}/n_i)$,

$q$ is electron charge,

$N_{sub}$ is the doping concentration of the substrate,

$Q_{dep}$ is the charge in the depletion region,

$C_{ox}$ is the gate oxide capacitance per unit area.
MOS I/V Characteristics: Threshold Voltage (2)

The PMOS device operates in the same manner as the NMOS device except that $V_{GS}$, $V_{DS}$ and the threshold voltage $V_T$ are negative. As the gate-source voltage becomes sufficiently negative, an inversion layer consisting of holes is formed at the oxide-silicon interface, providing a conduction path between the source and the drain.

- Formation of inversion layer

![PMOS device diagram](image)
Derivation of I/V Characteristics (1)

Channel charge density (charge per unit length)

\[ Q_d = WC_{OX} (V_{GS} - V_{TH}) \]

\[ Q_d (X) = WC_{OX} (V_{GS} - V(X) - V_{TH}) \]
Derivation of I/V Characteristics (2)

\[ I_D = -WC_{OX}(V_{GS} - V(X) - V_{TH})v \]

The negative sign is inserted in the above formula as the charge carriers are negative. Also \( v \) denotes the velocity of the electrons in the channel.

\[ I_D = WC_{OX}(V_{GS} - V(x) - V_{TH})\mu_n \frac{dV(x)}{dx} \]

\[ \int_{x=0}^{L} I_D dx = \int_{V=0}^{V_{DS}} WC_{OX}\mu_n(V_{GS} - V(x) - V_{TH})dV \]

\[ I_D = \mu_n C_{OX} \frac{W}{L} \left[ (V_{GS} - V_{TH})V_{DS} - \frac{1}{2} V_{DS}^2 \right] \]

Here \( L \) is the effective channel length.
Derivation of I/V Characteristics (3)

$$I_D = \mu_n C_{OX} \frac{W}{L} \left[ (V_{GS} - V_{TH})V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

Maximum drain current is given by:

$$I_{D,max} = \frac{1}{2} \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{TH})^2$$

If $V_{DS} \leq V_{GS} - V_{TH}$, the device operates in the “triode region.”
Derivation of I/V Characteristics (4)

If $V_{DS} \ll 2(V_{GS} - V_{TH})$ then

$$I_D \approx \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}$$

The drain current is a linear function of $V_{DS}$. The linear relationship implies that the path from the source to the drain can be represented by a linear resistor equal to

$$R_{on} = \frac{1}{\mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{TH})}$$

If $V_{DS} \ll 2(V_{GS} - V_{TH})$ the device operates in “deep triode region.”
Derivation of I/V Characteristics (5)

\[ V(x_1) = V_{GS} - V_{TH} \]

\[ V(x_2) = V_{GS} - V_{TH} \]

**Pinch-off behavior**
Derivation of I/V Characteristics (6)

\[ I_D = \frac{1}{2} \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{TH})^2 \]

With the approximation \( L \approx L' \)

a saturated MOSFET can be used as a current source connected between the drain and the source, an important component in analog design.

Fig: Saturation of drain current
Derivation of I/V Characteristics (7)

A MOSFET when operated in the saturation region acts as a voltage-controlled current source i.e. changes in the gate-to-source voltage gives rise changes in the drain current $I_D$. This is known as transconductance, $g_m$ which is expressed as:

$$g_m = \frac{dI_D}{dV_{GS}} \bigg|_{V_{DS}=\text{const}} = \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{TH})$$

g$_m$ can also be expressed as:

$$g_m = \sqrt{2}\mu_n C_{OX} \frac{W}{L} I_D = \frac{2I_D}{V_{GS} - V_{TH}}$$
Derivation of I/V Characteristics (8)

The above figures show MOS transconductance as a function of overdrive and drain current.
Transistor Second Order Effect, Body Effect

Fig: NMOS device with negative bulk voltage

Suppose $V_s=V_D=0$. If $V_B$ become more negative, more holes are attracted to the substrate.
Body Effect (1)

- For $V_B = 0$:
  - $V_G$ applied to gate, $V_D$ to drain.
  - Charge $Q_D$.
  - No significant body effect.

- For $V_B < 0$:
  - $V_G$ applied to gate, $V_D$ to drain.
  - Charge $Q_D$.
  - Significant body effect due to the drain biasing.
Ignoring body effect. As $V_{in}$ varies, $V_{out}$ closely follows the input because the drain current remains equal to $I_1$.

$$I_1 = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{out} - V_{TH})^2,$$

Now suppose the substrate is tied to ground and body effect is significant. As $V_{in}$ and hence $V_{out}$ become more positive, the potential difference between the source and the bulk increases, raising the value of $V_{TH}$. 
Channel-Length Modulation (1)
The actual length of the inverted channel gradually decreases as the potential difference between the gate and the drain increases. In saturation:

\[ I_D \approx \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}), \]

where \( \lambda \) is channel-length modulation coefficient, which represents the relative variation in length for a given increment in \( V_{DS} \).
Channel-Length Modulation (2)

With channel-length modulation, some of the expressions derived for $g_m$ must be modified.

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})(1 + \lambda V_{DS}).$$

$$g_m = \sqrt{\frac{2\mu C_{ox} (W/L)}{1 + \lambda V_{DS}}} I_D.$$

Since the dependence on $V_{DS}$ is much weaker, the drain-source voltage is not used to set the current.
Subthreshold Condition (1)

In reality for $V_{GS} \approx V_{TH}$ a “weak” inversion layer still exists and some current flows from D to S. Even for $V_{GS} < V_{TH}$, $I_D$ is finite, but it exhibits an exponential dependence on $V_{GS}$ called “sub-threshold conduction”. This effect can be formulated for $V_{DS}$ greater than roughly 200 mV as

$$I_D = I_0 \exp \frac{V_{GS}}{\zeta V_T},$$

where $\zeta > 1$ is the nonideality factor and $V_T = kT/q$. 
Subthreshold Condition (2)

- As the $V_{GS}$ falls below $V_{TH}$, the drain current drops at a finite rate. With typical values of $\zeta$, at room temperature $V_{GS}$ must decrease by approximately 80 mV for $I_D$ to decrease by one decade.
- The exponential dependence of $I_D$ upon $V_{GS}$ in subthreshold operation may suggest the use of MOS device in this regime so as to achieve a higher gain.

MOS subthreshold characteristics
Voltage Limitations

- MOSFETs experience various breakdown effects if their terminal voltage differences exceed certain limits.
- At high gate-source voltages, the gate oxide breaks down damaging the transistor.
- In short-channel devices, an excessively large drain-source voltage widens the depletion region around the drain, creating a very large drain current (the effect is called “punch through”)

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Small-Signal Model (1)

- Conductance
- Transconductance and body effect transconductance
- Small signal gain
- Capacitances of a transistor
Small-Signal Model (2)

Derived by producing a small increment in a bias point and calculating the resulting increment in other bias parameters. Since the drain current is a function of the gate-source voltage, a voltage-dependent current source equal to $g_m V_{GS}$ is incorporated. The low-frequency impedance between G and S is very high.

![Small-signal model of an ideal MOSFET](image-url)
Small-Signal Model (3)

The drain current also varies with the drain-source voltage. This effect can also be modeled by a voltage-dependent current source.
Small-Signal Model (4)

Tied between D and S, the resistor is given by:

\[
 r_0 = \frac{dV_{DS}}{dl_D} = \frac{1}{dI_D/dV_{DS}} = \frac{1}{\frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \lambda} \approx \frac{1}{\lambda l_D}
\]
Small-Signal Model (5)

The bulk potential influences the threshold voltage and hence the gate-source overdrive. The drain current is a function of the bulk voltage (the bulk behaves as a second gate). Modeling this dependence by a current source connected between D and S, the value can be written as $g_{mb}V_{BS}$.
Small-Signal Model (6)

In saturation region, $g_{mb}$ can be expressed as:

$$g_{mb} = \frac{dI_D}{dV_{BS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \left( -\frac{dV_{TH}}{dV_{BS}} \right)$$

Also

$$\frac{dV_{TH}}{dV_{BS}} = -\frac{dV_{TH}}{dV_{SB}} = -\frac{\gamma}{2} (2\phi_F + V_{SB})^{-1/2}$$

Thus

$$g_{mb} = g_m \frac{\gamma}{2\sqrt{2}\phi_F + V_{SB}} = \eta g_m$$

As expected, $g_{mb}$ is proportional to $\gamma$. Last equation also suggests that incremental body effect becomes less pronounced as $V_{SB}$ increases. $g_m V_{GS}$ and $g_{mb} V_{BS}$ have the same polarity, i.e., raising the gate voltage has the same effect as raising the bulk potential.
Capacitances of Transistor

The complete small-signal model also includes the device capacitances.
Single Stage Amplifiers
Common Source Stage

\[ V_{out} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{th})^2 \]

\[ A_v = \frac{\partial V_{out}}{\partial V_{in}} = -R_D \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{th}) = -g_m R_D \]
CS Stage with Diode Connected Load (1)

Diode-connected NMOS and PMOS devices

Small signal equivalent circuit
CS Stage with Diode Connected Load (2)

Arrangement for measuring the equivalent resistance of a diode-connected MOSFET
CS stage with Diode Connected Load (3)

\[ A_v = -G_{ml} \frac{1}{G_m + G_{mb2}} = -G_{ml} \frac{1}{G_{m2}} \frac{1}{1 + \eta} \]
CS stage with Diode Connected Load (4)

\[ A_v = \frac{G_{m1}}{G_{m2}} \]
**CS Stage with Current-Source Load**

\[ A_v = -g_m R_D = -g_m \left( r_{01} \parallel r_{02} \right) \]

\[ g_m r_{01} = \sqrt{2 \cdot \frac{w}{l} \mu_n C_{ox} l_d \frac{1}{\lambda l_D}} \]
CS Stage with Triode Load

\[ V_{\text{outmax}} = V_{DD} \]
CS Stage with Source Degeneration

\[ G_m = \frac{g_m}{1 + g_m R_s} \]

\[ A_v = -G_m R_D = \frac{-g_m R_D}{1 + g_m R_s} \]
Small-signal Equivalent Circuit of a Degenerated CS Stage
Source Follower (1)

Source follower

Its input-output characteristic

Input-output characteristic can be expressed as:

$$\frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left(V_{in} - V_{TH} - V_{out}\right)^2 R_S = V_{out}$$
Source Follower (2)

Calculate the small-signal gain of the circuit by differentiating both sides with respect to \( V_{in} \)

\[
\frac{1}{2} \mu_n C_{ox} \frac{W}{L} 2(V_{in} - V_{TH} - V_{out}) \left(1 - \frac{\partial V_{TH}}{\partial V_{in}} - \frac{\partial V_{out}}{\partial V_{in}}\right) R_S = \frac{\partial V_{out}}{\partial V_{in}}
\]

Since \( \frac{\partial V_{TH}}{\partial V_{in}} = \eta \frac{\partial V_{out}}{\partial V_{in}} \),

\[
\frac{\partial V_{out}}{\partial V_{in}} = \frac{\frac{1}{2} \mu_n C_{ox} \frac{W}{L} 2(V_{in} - V_{TH} - V_{out}) R_S}{1 + \frac{1}{2} \mu_n C_{ox} \frac{W}{L} 2(V_{in} - V_{TH} - V_{out}) R_S (1 + \eta)}
\]

Also note that

\[ g_m = \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH} - V_{out}) \]

Consequently,

\[ A_v = \frac{g_m R_S}{1 + (g_m + g_{mb}) R_S} \]
Source Follower (3)

The result is more easily obtained with the aid of a small-signal equivalent circuit. \( V_{\text{in}} - V_1 = V_{\text{out}}, V_{bs} = -V_{\text{out}} \), and \( g_m V_1 - g_{mb} V_{\text{out}} = \frac{V_{\text{out}}}{R_s} \) are obtained below:

\[
\begin{align*}
V_{\text{out}} &= g_m V_1 - g_{mb} V_{bs} \\
\text{Small-signal equivalent circuit of source follower}
\end{align*}
\]

\[
\begin{align*}
\text{Source follower using an NMOS transistor as current source}
\end{align*}
\]
Source Follower with NMOS transistor as current source (1)

To gain a better understanding of source followers, calculate the small-signal output resistance of the circuit. Using the equivalent circuit and $V_1 = -V_x$:

$$I_x - g_m V_x - g_{mb} V_x = 0$$
**Source Follower with NMOS transistor as Current Source (2)**

**Fig:** Calculation of the output impedance of a source follower

\[ R_{\text{out}} = \frac{1}{g_m + g_{mb}} \]
Source Follower with NMOS transistor as Current Source (3)

The magnitude of the current source $g_{mb} V_{bs}$ is linearly proportional to the voltage across it. Such behaviour is that of a simple resistor equal to $1/g_{mb}$, yielding the small-signal model.

$$\text{Fig: Source follower including body effect}$$

Without $1/g_{mb}$, the output resistance equals $1/g_m$, concluding that

$$R_{out} = \frac{1}{g_m} \parallel \frac{1}{g_{mb}} = \frac{g_m + g_{mb}}{g_m g_{mb}}$$
Source Follower with NMOS transistor as current source (4)

Fig: Representation of intrinsic source follower by a Thevenin equivalent

\[ A_v = \frac{1}{\frac{1}{g_{mb}} + \frac{1}{g_m + g_{mb}}} = \frac{g_m}{g_{mb} + g_m} \]
Source Follower with NMOS transistor as Current Source (5)

\[
A_v = \frac{1}{g_{mb} \parallel r_{O1} \parallel r_{O2} \parallel R_L} - \frac{1}{g_{mb} \parallel r_{O1} \parallel r_{O2} \parallel R_L + \frac{1}{g_m}}
\]

Small-signal equivalent circuit  
Source follower driving load resistance
Source Follower with NMOS Transistor as Current Source (6)

Fig: PMOS source follower with no body effect
Source Follower with NMOS transistor as Current Source (7)

Fig: Cascode of source follower & CS stage
The load can be driven by a source follower with an overall voltage gain of
\[
\frac{V_{\text{out}}}{V_{\text{in}}} |_{\text{SF}} \approx \frac{R_L}{R_L + \frac{1}{g_{ml}}}
\]

The load can be included as part of a common source stage proving a gain of
\[
\frac{V_{\text{out}}}{V_{\text{in}}} |_{\text{CS}} \approx -g_{ml}R_L
\]
Common-Gate Stage (1)

Assume that $V_{in}$ decreases from a large positive value. For $V_{in} \geq V_b - V_{TH}$, $M_1$ is off and $V_{out} = V_{DD}$.

For lower values of $V_{in}$:

$$I_D = \frac{1}{2} \mu_n C_{OX} \frac{W}{L} (V_b - V_{in} - V_{TH})^2$$

if $M_1$ is in saturation, as $V_{in}$ decreases, so does $V_{out}$ eventually driving $M_1$ into the triode region.
Common-Gate Stage (2)

\[ V_{DD} - \frac{1}{2} \mu_n C_{OX} \frac{W}{L} (V_b - V_{in} - V_{TH})^2 R_D = V_b - V_{TH} \]

If \( M_1 \) is saturated, the output voltage can be expressed as

\[ V_{out} = V_{DD} - \frac{1}{2} \mu_n C_{OX} \frac{W}{L} (V_b - V_{in} - V_{TH})^2 R_D \]

Fig: Common-gate input-output characteristic
Common-Gate Stage (3)

Obtaining a small-signal gain of

\[
\frac{\partial V_{\text{out}}}{\partial V_{\text{in}}} = -\mu_n C_{\text{OX}} \frac{W}{L} (V_b - V_{\text{in}} - V_{\text{TH}}) \left( -1 - \frac{\partial V_{\text{TH}}}{\partial V_{\text{in}}} \right) R_D
\]

Since \( \frac{\partial V_{\text{TH}}}{\partial V_{\text{in}}} = \frac{\partial V_{\text{TH}}}{\partial V_{\text{SB}}} = \eta \) the following is obtained

\[
\frac{\partial V_{\text{out}}}{\partial V_{\text{in}}} = \mu_n C_{\text{OX}} \frac{W}{L} (V_b - V_{\text{in}} - V_{\text{TH}})(1 + \eta) R_D = g_m (1 + \eta) R_D
\]

The gain is positive. Interestingly, body effect increases the equivalent transconductance of the stage.

The circuit can be analyzed with the aid of its equivalent. Noting that the current flowing through \( R_S \) is equal to \(-V_{\text{out}}/R_D\), this is obtained:

\[
V_1 - \frac{V_{\text{out}}}{R_D} R_S + V_{\text{in}} = 0
\]
Common-Gate Stage (4)

Since the current through $r_O$ is equal to $-V_{out}/R_D-g_mv_1-g_mbV_1$, it can be written

$$r_O\left(\frac{-V_{out}}{R_D} - g_m V_1 - g_mb V_1\right) - \frac{V_{out}}{R_D}R_S + V_{in} = V_{out}$$

Upon substitution for $V_1$,

$$r_O\left[\frac{-V_{out}}{R_D} - (g_m + g_mb)\left(V_{out}\frac{R_S}{R_D} - V_{in}\right)\right] - \frac{V_{out}R_S}{R_D} + V_{in} = V_{out}$$
Common-Gate Stage (5)

It follows that

\[
\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{(g_m + g_{mb})r_O + 1}{r_O + (g_m + g_{mb})r_O R_S + R_S + R_D} R_D
\]

The gain of the common-gate stage is slightly higher due to body effect.

The input resistance of a CG stage is slightly higher due to body effect.

\[
V_1 = -V_X \text{ and the current through } r_O \text{ is equal to } I_X + g_m V_1 + g_{mb} V_1 = I_X - (g_m + g_{mb})V_X, \text{ the voltages can be added up across } r_O \text{ and } R_D \text{ as }
\]

\[
R_D I_X + r_O [I_X - (g_m + g_{mb})V_X] = V_X
\]

Thus,

\[
\frac{V_X}{I_X} = \frac{R_D}{1 + (g_m + g_{mb})r_O} \approx \frac{R_D}{(g_m + g_{mb})r_O} + \frac{1}{g_m + g_{mb}}
\]
Common-Gate Stage (6)

First suppose $R_D = 0$. Then,

$$\frac{V_X}{I_X} = \frac{r_O}{1 + (g_m + g_{mb})r_O} = \frac{1}{r_O + g_m + g_{mb}}$$

The input impedance of a common-gate stage is relatively low only if the load impedance connected to the drain is small.

In order to calculate the output impedance of the common-gate stage,

$$R_{out} = \frac{1}{[1+(g_m+g_{mb})r_O]R_S+r_O}||R_D},$$

$$++(3.13)>>$$

$$A_v = (g_m+g_{mb})r_O + 1$$

*Fig: Input resistance of CG stage with ideal current source load*
Common-Gate Stage (7)

Fig: Calculation of output resistance of a CG stage
M₁ generates a small-signal drain current proportional to Vᵢₙ & M₂ simply rules the current to Rₓ.

Cascode Stage (1)

Cascode stage

Allowed voltages in cascode stage.
Cascode Stage (2)

As $V_{in}$ exceeds $V_{TH1}$, $M_1$ begins to draw current, and $V_{out}$ drops. Since $I_{D2}$ increases, $V_{GS2}$ must increase as well, causing $V_X$ to fall.

**Input-output characteristic of a cascode stage**

**Small-signal equivalent circuit of cascode stage**
An important property of the cascode structure is its high output impedance. To calculate $R_{out}$, the circuit can be viewed as a common-source stage with a degeneration resistor equal to $r_{o1}$. Thus,

$$R_{out} = [1+(g_{m2}+g_{mb2})r_{o2}]r_{o1}+r_{O2}$$
Cascode Stage (4)

If both $M_1$ & $M_2$ operate in saturation, then $G_m \approx g_{m1}$ & $R_{out} \approx (g_{m2}+g_{mb2})r_{O1}r_{O2}$, yielding

$$A_v = (g_{m2}+g_{mb2})r_{O2}g_{mb1}r_{O1}$$

Cascode stage with current-source load

Increasing output impedance by increasing the device length or cascoding.

Now consider the output impedance achieved in each case. Since

$$g_m r_O = \sqrt{2\mu_n C_{ox} \frac{W}{L}} I_D \frac{1}{\lambda I_D}$$
Cascode Stage (5)

If the gate bias voltages are chosen properly, the maximum output swing is equal to

\[ V_{dd} - (V_{GS1} - V_{TH1}) - (V_{GS2} - V_{TH2}) - |(V_{GS3} - V_{TH3})| - |(V_{GS4} - V_{TH4})| \]

Substituting \( G_m \approx g_{m1} \) & \( R_{out} = \{ [1+(g_{m2}+g_{mb2})r_{o2}]r_{O1}+r_{O2} \} \parallel \{ [1+(g_{m3}+g_{mb3})r_{o3}]r_{O4}+r_{o3} \} \)

\[ |A_v| \approx g_{m1} R_{out} \] is obtained. For typical values, the voltage gain is approximated as

\[ |A_v| \approx g_{m1} [(g_{m2}r_{o2}r_{O1})\parallel(g_{m3}r_{o3}r_{O4})] \]

As \( V_x \) falls below \( V_{b2} - V_{TH2} \), \( M_2 \) requires a larger gate-source overdrive so as to sustain the current drawn by \( M_1 \).

\[ I_{D2} = \frac{1}{2} \mu_n C_{OX} \left( \frac{W}{L} \right) [2(V_{b2} - V_P - V_{TH2})(V_X - V_P) - (V_X - V_P)^2] \]
Folded Cascode (1)

For $V_{in} > V_{dd} - |V_{TH1}|$, $M_1$ is off & $M_2$ carries all of $I_1$ (if $I_1$ is excessively large, $M_2$ may enter deep triode region, possibly driving $I_1$ into the triode region as well), yielding $V_{out} = V_{DD} - I_1R_D$. For $V_{in} < V_{DD} - |V_{TH1}|$, $M_1$ turns on in saturation, giving

$$I_{D2} = I_1 - \frac{1}{2} \mu_p C_{OX} \left(\frac{W}{L}\right)_1 (V_{DD} - V_{in} - |V_{TH1}|)^2$$
Folded Cascode (2)

As $V_{in}$ drops, $I_{D2}$ decreases further falling to zero if $I_{D1}=I_1$. For this to occur:

$$\frac{1}{2} \mu_p C_{OX} \left( \frac{W}{L} \right)_1 (V_{DD} - V_{in} - |V_{TH1}|^2) = I_1$$

Thus,

$$V_{inl} = V_{DD} - \sqrt{\frac{2I_1}{\mu_p C_{OX} \left( \frac{W}{L} \right)_1}} - |V_{TH1}|$$

Large-signal characteristics of folded cascode
Session summary

- Small signal model of MOS transistor consists of voltage controlled current source, drain to source resistance, bulk controlled voltage source
- Capacitances of MOS introduce delay
- CS is used for voltage amplification, CD is used as voltage follower and CG is used as impedance matching network
- In design of Opamp, phase margin should be 60 degrees for good stability